

RESPONSE UNDER 37 C.F.R. § 1.111
U.S. APP. NO. 09/485,443

Summary of the Invention

The present invention relates to a method of optimizing the topology of a serial bus having a plurality of nodes, each of the nodes having one or more communication ports. According to one aspect of the invention, the nodes are prioritized according to the number of ports of the nodes and the transmission speed of the nodes. For example, the nodes shown in Figure 3A may be prioritized as shown in Figure 3B, with priority decreasing along the arrow connecting points A and B. In the example, the node to the far left of Figure 3B has a speed of 400 Mbps, followed by two nodes having speeds of 200 Mbps and three nodes having speeds of 100 Mbps. The three nodes having speeds of 100 Mbps are arranged in order of priority based upon the number of ports contained therein. Thus, the node having a speed of 100 Mbps and three ports has a priority higher than the node having a speed of 100 Mbps and two nodes.

This aspect of the invention also includes a step of connecting a non-used port of the node of the lowest priority with a port of the node of the second next priority, and repeating the connecting step until all of the nodes are connected together, whereby the nodes are connected through the ports according to priority number. This results in a bus topology such as shown in Figure 3E.

According to another aspect of the invention, in certain situations, the priority of the nodes described above must be rearranged in order to accomplish a complete connection of all of the nodes. For example, prioritizing the nodes shown in Figure 4A according to the above-described technique results in the priority shown in Figure 4B. Connecting the nodes in the manner described above results in a bus topology shown in Figure 4D in which there are no

RESPONSE UNDER 37 C.F.R. § 1.111
U.S. APP. NO. 09/485,443

connections for two of the nodes. Accordingly, when all of the ports of the node of higher priority are used, the last connected node is separated and the node of the next priority is substituted for the last connected node. Thus, the priority is rearranged as shown in Figure 4D, and the resulting bus topology is shown in Figure 4F.

Analysis of the Claim Rejection

In rejecting claims 1-5 as being unpatentable over Klein, the Examiner cites Klein as disclosing a bus system accommodating both high speed and low speed devices. The Examiner admits that Klein does not disclose a serial bus, but takes official notice of the following:

“1. Due to the serial bus’ design and physical restriction, it is inherent that a child node’s performance can be affected or undercut by the transmission speed of its parent node and nodes in the hopping path. The common industrial local bus design teaches that it is ideal to place the higher-speed devices closer to the CPU because the CPU is where the instructions are initiated and it reduces the transmission latency. Analogously, it would be obvious to one in the computer art to connect higher-speed devices closer to the serial bus connector because the serial bus connector is where the serial bus’ instructions are initiated, and this arrangement will also minimize the parent nodes’ effect on the child nodes’ performance due to various transmission speed. In addition, the number of ports of each device has an inherent effect on overall system performance. The number of ports correlates to the maximum number of child nodes, such that more child

RESPONSE UNDER 37 C.F.R. § 1.111
U.S. APP. NO. 09/485,443

nodes can be connected closer to the serial bus connector and it avoids the child nodes' extra hops if they were connected further down in a serial bus."

Applicant respectfully disagrees with the Examiner's analysis for several reasons. First, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *In re Fine*, 837 F2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). This burden can only be satisfied by an objective teaching in the prior art or by cogent reasoning that the knowledge is available to one of ordinary skill in the art. *See In re Lalu*, 747 F2d 703, 223 USPQ 1257 (Fed. Cir. 1984). Furthermore, an Examiner may not rely on official or judicial notice at the exact point where patentable novelty is argued, but must come forward with pertinent prior art. *See Ex parte Cady*, 148 USPQ 162 (Pat. Off. Bd. App. & Inter. 1965). Thus, the Examiner's reliance upon official notice should not be maintained since the Examiner has taken official notice on issues where patentable novelty is asserted.

Second, Applicant respectfully submits that the Examiner's analysis amounts to hindsight reconstruction of the art in view of Applicant's own disclosure. Claim 1 recites three steps:

"prioritizing said nodes according to the number of said ports and the transmission speed of said nodes;

connecting a non-used port of the node of the lowest priority with a port of the node of the next priority; and

RESPONSE UNDER 37 C.F.R. § 1.111
U.S. APP. NO. 09/485,443

repeating the connecting step until all of said nodes are connected together, whereby said nodes are connected through said ports according to priority order."

In order to render this combination of steps obvious, the Examiner cites Klein which merely shows combining a low speed communications bus and a high speed communications bus into a single multiplexed communications bus that supports both low speed and high speed operations. There is no teaching or suggestion in this reference for any of the above quoted steps of claim 1. To make up for the deficiencies of Klein, the Examiner takes official notice of various matters and provides a hindsight reconstruction of Klein and the matters taken by official notice to argue that the invention of claim 1 is obvious. Applicant respectfully requests the Examiner to provide references showing each of the matters for which he takes official notice and to provide cogent reasoning as to why the references should be combined in the manner suggested by the Examiner.

Third, even if the Examiner's official notices are accurate, Applicant respectfully submits they are not properly combined with Klein to reject the present invention. References cannot properly be combined with each other when such would result in destroying that on which the invention of one of the references is based. *Ex parte Hartmann*, 186 USPQ 366, 367 (Pat. Off. Bd. App. & Inter. 1974). As mentioned above, Klein is directed to a method for combining a low-speed communications bus and a high-speed communications bus into a single multiplexed communications bus that supports both low-speed and high-speed operations. At one level of time multiplexing, both data and addresses are transmitted over a common set of signal lines. At

RESPONSE UNDER 37 C.F.R. § 1.111
U.S. APP. NO. 09/485,443

a second level of time multiplexing, both low-speed and high-speed bus operations are conducted over the shared data and address signal lines. See column 4, lines 12-16. Thus, the invention of Klein is not intended to be used with a serial bus. Modifying Klein according to the Examiner's suggestion based on official notice, would destroy that on which Klein is based. That is, converting the device of Klein to operate with a serial bus would destroy that on which Klein is based.

Additionally, the Klein '425 patent discloses two types of devices, one for low speed communication and another for high speed communication, which exist separately, and suggests a method for multiplexing a bus over shared time multiplexed control, using a bus arbiter. According to the operation of the Klein '245 patent, the performances of the devices are improved by locating a cache and a memory to be adjacent to a CPU. On the contrary, the IEEE 1394 serial bus does not have dependent relation different from the construction of a general computer and also all the devices can order a command. Moreover, each device checks whether a bus is busy or not and then transmission can be performed within a predetermined time period. In view of the foregoing, the fact that a device for a high speed communication is located adjacent to the CPU, suggested by the Klein '245 patent, cannot be applied to the IEEE 1394 serial bus of the present invention.

Further, in terms of a construction of a bus topology, the present invention discloses that after being compared in relation to a node device's speed and the number of ports, priority may be given to the faster device and the ports including the higher number and thus a device having the higher speed can be connected to the greater number of devices. The IEEE 1394 device

RESPONSE UNDER 37 C.F.R. § 1.111
U.S. APP. NO. 09/485,443

determines a transmission rate depending on a lower speed device when there is a lower speed device between two nodes to be transmittable. As stated above, the present invention determines priority in order for a high speed device to be connected to a lot of nodes. In other words, the high speed device is the center point of the bus topology.

Herein, the performance of the bus is dependent on the speed of the node because there is uncertainty as to how many ports can be connected thereto until a bus is completed. However, there is some difficulty in constructing a bus if only the speed of a node is considered. Therefore, the bus topology should be determined in consideration of both the node's speed and the number of ports.

Furthermore, Applicant cannot find any example of an extremely large scale bus is implemented using the IEEE 1394. In this regard, at the most, four or five nodes may be used therefor. In this case, however, if the topology should not be constructed just like the present invention, there may be difficulty in the construction of the bus and deterioration of performance thereof.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

RESPONSE UNDER 37 C.F.R. § 1.111
U.S. APP. NO. 09/485,443

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Respectfully submitted,



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